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(54) **An integratable voltage comparator with reduced offset**

(57) A comparator wherein the voltages on the inputs (12, 13) are converted to currents (1, 6, 16) for supply to active loads. Following the application of the two voltages whose difference is to be measured a common input voltage equal to the mean or some other function of the two voltages is applied. The change in voltage at the active loads brought about by the substitution is used to provide an offset corrected output.

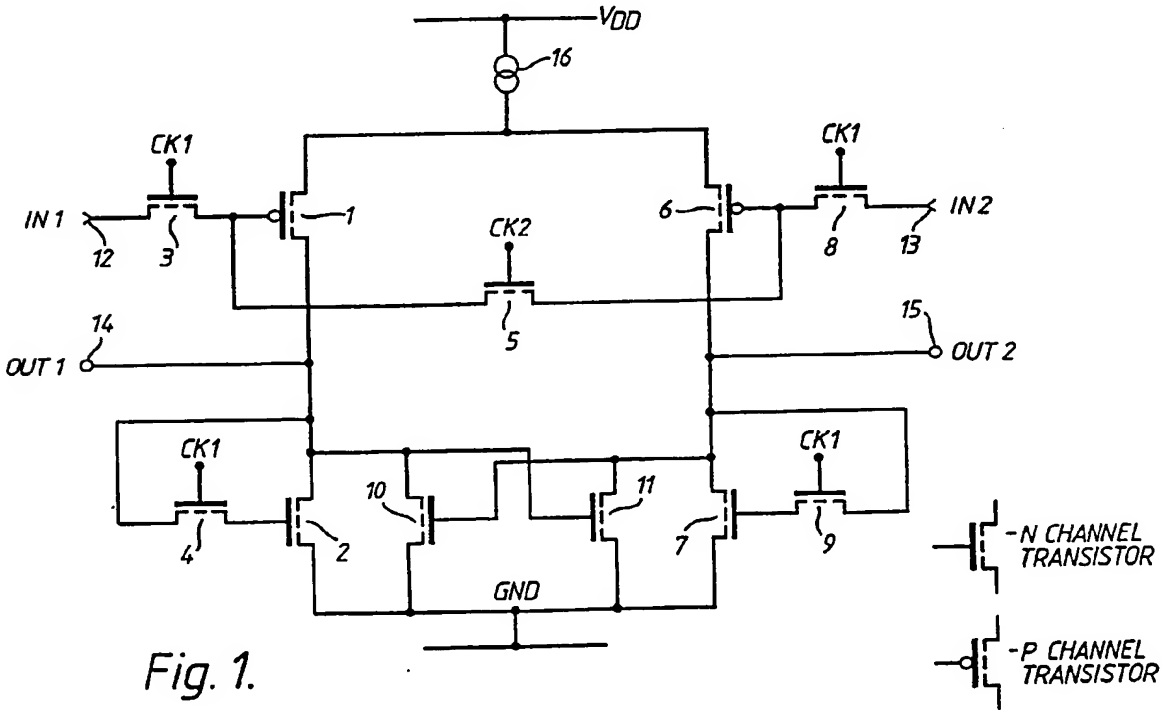

Fig. 1.

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

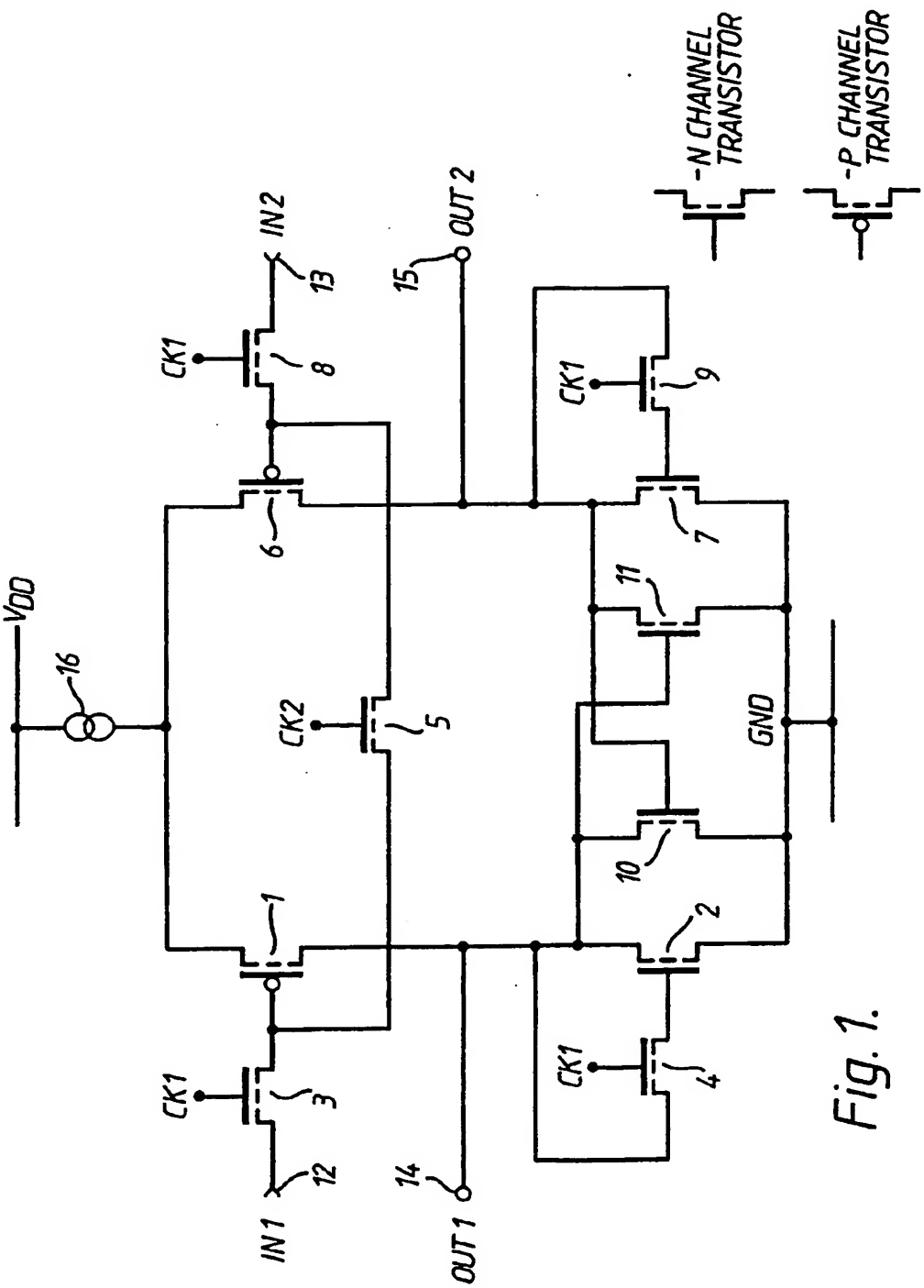
VDD
16
CK1
CK2
CK1
CK1
CK1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
IN1
IN2
OUT1
OUT2
GND
-N CHANNEL TRANSISTOR
-P CHANNEL TRANSISTOR

Fig. 1.

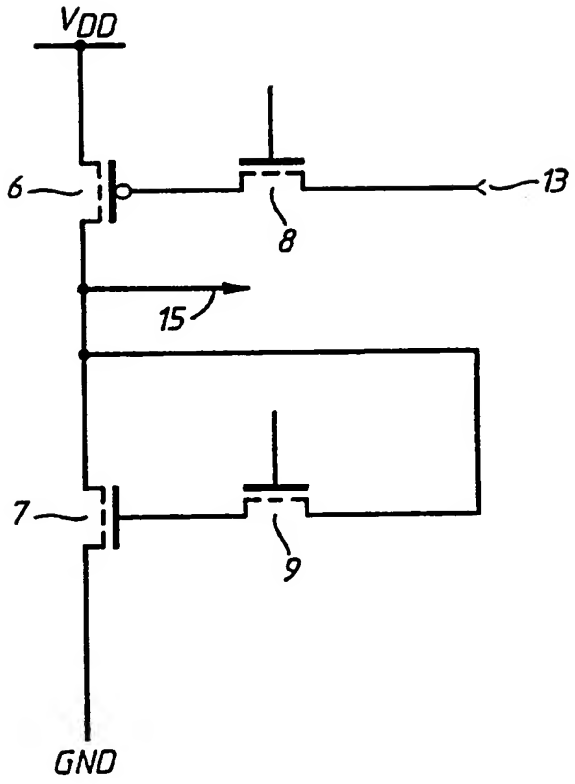

Fig. 2.

A Voltage Comparator

The present invention relates to a voltage comparator.

The function of a voltage comparator is to provide an indication of which of two voltages applied to respective input ports of the voltage comparator is the larger.

An object of the present invention is the provision of a voltage comparator which is especially suitable for fabrication as an integrated circuit.

The present invention provides a voltage comparator which is operable to provide an output signal indicating which of two voltages applied to its input ports is the greater, by the steps of:

generating, by means of voltage-to-current converters, respective first and second currents corresponding to the two applied voltages,

applying the first and second currents to respective active loads which are capable of being set to maintain operation at those currents,

setting the active loads to maintain operation at the first and second currents,

applying to the voltage-to-current converters, in place of the two applied voltages, a common input voltage that is the mean of the two applied voltages,

generating substantially equal currents correspond-

ing to the common input voltage,

applying the substantially equal currents to the active loads in place of the first and second currents, the active loads being set to conduct the first and second currents, and

providing an output signal indicating the sense of any voltage change occurring at the active loads when the substantially equal currents are applied in place of the first and second currents.

The voltage comparator is capable of providing a substantial reduction in offset voltage compared with conventional voltage comparators without storing any offset voltage by means of a capacitor.

Preferably, a regenerative switching circuit is connected between the active loads for providing an output signal indicating the sense of any voltage change occurring at the active loads when the substantially equal currents are applied in place of the first and second currents.

Preferably, the regenerative switching circuit is a bistable latch circuit.

Preferably, the bistable latch circuit consists of a first and a second insulated gate field effect transistor (IGFET), the gate electrode of the first IGFET being connected to the drain electrode of the second IGFET and to one of the active loads, and the gate electrode of the second IGFET being connected to the drain electrode of

the first IGFET and to the other active load.

Preferably, each active load is a voltage-controlled current sink that is operable, first, to generate its own control voltage in order to conduct a current applied to it, and is then operable in a state in which it stores and responds only to the control voltage generated while it conducted the applied current.

Preferably, the voltage-controlled current sink includes an IGFET which has its gate electrode connectible to its drain electrode by way of a switch means.

One arrangement of the voltage comparator has a first input port connectible to a control port of a first voltage-to-current converter by way of first switch means, a second input port connectible to a control port of a second voltage-to-current converter by way of second switch means, the control ports of the voltage-to-currrent converters being capable of storing charge and being connectible together by third switch means, in operation, the first and second currents being generated with the third switch means non-conductive and the first and second switch means conductive, and the substantially equal currents being generated with the third switch means conductive and the first and second switch means non-conductive.

Each active load utilised by the comparator is switchable between a first state in which it sinks a

current supplied to it by adjusting its control voltage until its current is the same as the current supplied, and a second state in which the active load "remembers" the current supplied to it and maintains operation at that current by storing and responding only to the control voltage which it developed in the first state.

The present invention provides, also, a circuit arrangement including a voltage-to-current converter connected to supply current to an active load, wherein the active load is a voltage-controlled current sink operable, first, to generate its own control voltage in order to conduct a current applied to it, and is then operable in a state in which it stores and responds only to the control voltage generated while it conducted the applied current.

Preferably, the voltage-controlled current sink includes an IGFET which has its gate electrode connectible to its drain electrode by way of a switch means. In operation, the switch means is conductive in order for the IGFET to generate its own control voltage and conduct the applied current, and the switch means is non-conductive in order for the IGFET to "remember" that current.

A voltage comparator, in accordance with one aspect of the present invention, and a circuit arrangement, forming a part of the voltage comparator, in accordance with a further aspect of the present invention, will now

be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a circuit diagram representing the voltage comparator, and

Fig. 2 is a circuit diagram representing the circuit arrangement.

Referring to Fig. 1 of the accompanying drawings, the voltage comparator includes a first voltage-to-current converter consisting of a P-channel enhancement mode insulated gate field effect transistor (IGFET) 1, which is connected to an active load consisting of a first N-channel enhancement mode IGFET 2 connected drain electrode to drain electrode with the P-channel IGFET 1, and a second N-channel enhancement mode IGFET 4 the drain electrode of which is connected to the drain electrode of the first N-channel IGFET 2 and the source electrode of which is connected to the gate electrode of the first N-channel IGFET 2. A third IGFET 3 has its source electrode connected to the gate electrode of the IGFET 1.

Referring to Fig. 1, the voltage comparator includes a second voltage-to-current converter consisting of a second P-channel IGFET 6 which is connected drain electrode to drain electrode with a fourth N-channel IGFET 7, a fifth N-channel IGFET N-channel IGFET 9 the drain electrode of which is connected to the drain electrode of the N-channel IGFET 7 and the source

electrode of which is connected to the gate electrode of the N-channel IGFET 7. A sixth IGFET 8 has its source electrode connected to the gate electrode of the IGFET 6. All of the IGFETS are enhancement mode devices.

Referring to Fig. 1, the voltage comparator includes a seventh N-channel IGFET 5 the drain electrode of which is connected to the gate electrode of the N-channel IGFET 6 and the source electrode of which is connected to the gate electrode of the N-channel IGFET 1. The connections of the N-channel IGFET 5 to the IGFETs 1 and 6 can be reversed.

Referring to Fig. 1, an eighth N-channel IGFET 10 is connected in parallel with the N-channel IGFET 2, drain electrode to drain electrode and source electrode to source electrode, and the gate electrode of the eighth N-channel IGFET 10 is connected to the drain electrode of the N-channel IGFET 7. A ninth N-channel IGFET 11 is connected in parallel with the N-channel IGFET 7, drain electrode to drain electrode and source electrode to source electrode, and the gate electrode of the transistor 11 is connected to the drain electrode of the N-channel IGFET 2. The source electrodes of the N-channel IGFETs 2, 7, 10 and 11 are connected together. The N-channel IGFETs 10 and 11 form a bistable latch connected between the drain electrodes of the N-channel IGFETs 2 and 7. The source electrodes of the N-channel IGFETs 1 and 6 are connected together. Current is

supplied to the IGFETS 1 and 6 by way of a current source 16.

Referring to Fig. 1, the voltage comparator has a first input port 12 which is the drain electrode of the N-channel IGFET 3, a second input port 13 which is the drain electrode of the N-channel IGFET 8, a first output port 14 which is the common connection of the drain electrodes of the N-channel IGFETs 2, 4 and 10, and a second output port 15 which is the common connection of the drain electrodes of the N-channel IGFETs 7, 9 and 11. The voltage comparator has, also, a positive voltage supply port which is connected to the current source 16, and a negative voltage supply port which is the common connection of the source electrodes of the N-channel IGFETs 2, 7, 10 and 11.

The voltage comparator represented by Fig. 1 has two operating states.

When the voltage comparator of Fig. 1 is in the first operating state the N-channel IGFETs 3, 4, 8 and 9 are in their conductive state and the N-channel IGFET 5 is in its non-conductive state. Input voltages IN1 and IN2 applied to the input ports 12 and 13, respectively, are transmitted to the gate electrodes of the P-channel IGFETs 1 and 6, respectively, causing them to be conductive. In the case of the P-channel IGFET 1, current flows in its drain electrode, and the gate electrode of the N-channel IGFET 2 is charged by current

reaching it by way of the N-channel IGFET 4. The charge established on the gate electrode of the N-channel IGFET 2 causes it to conduct and the IGFETs 1 and 2, together, establish a condition of dynamic equilibrium between their common drain currents and drain voltage, the gate voltage of the N-channel IGFET 2 being the same as its drain voltage by virtue of the connection of its drain electrode to its gate electrode by means of IGFET 4. The common drain current of the IGFETs 1 and 2 is dependent on the input voltage IN1. The IGFET 1 acts as a voltage to current converter. The IGFET 2, with the IGFET 4 conductive, acts as a current-to-voltage converter with its gate voltage such as to produce the required current. When the IGFET 4 is made non-conductive, the IGFET 2 continues to pass the current set up previously by virtue of the charge stored on its gate capacitance.

With the voltage comparator of Fig. 1 in the first operating state, the N-channel IGFETs 6 and 7 behave in a manner similar to the N-channel IGFETs 1 and 2, so the N-channel IGFETs 6 and 7, also, conduct a drain current dependent on the input voltage, which is IN2 in this case.

With the voltage comparator of Fig. 1 in the first operating state, if IN1 and IN2 are unequal, and say, IN1 is less than IN2, the drain voltage of the IGFETs 1 and 2 is higher than the drain voltage of the IGFETs 6 and 7.

The difference between the two drain voltages is applied to the N-channel IGFETs 10 and 11 which become conductive but are unable to act as a bistable latch because the IGFETs 2 and 7 act as heavy loads which reduce the gain of the cross-connected IGFETs 10 and 11.

Referring to Fig. 1, with the voltage-to-current converter IGFETs 1 and 6 conducting currents dependent on the voltages IN1 and IN2, the N-channel IGFETs 3, 4, 8 and 9 are changed to their non-conductive state without affecting the currents flowing in the active loads 2 and 7, since the gate electrodes of the IGFETs 1, 2, 6 and 7 act as stores for the gate signals which give rise to the drain currents. That is, the IGFETs 1, 2, 6 and 7 are able to "remember" their respective conditions and to maintain their drain currents at the previous levels.

Referring to Fig. 1, the voltage at the output port 15 relative to that at the output port 14 indicates which of the input voltages IN1 and IN2 is the larger. However, the voltages present at the output ports 14 and 15 include an offset voltage caused by differences between the devices used in the voltage comparator, resulting in the two sides of the voltage comparator not being identical to each other and there being a small imbalance between the two sides of the circuit. More specifically, if the output voltages from the voltage comparator are OUT 1 and OUT 2, then;

OUT 1 - OUT 2 = -gain (IN1 - IN2 + OFFSET,) assuming

that both voltage-to-current converters have substantially the same gain.

Referring to Fig. 1, an output signal with a substantially reduced offset voltage can be obtained by a change in the voltage comparator to its second operating state, which requires that the N-channel IGFET 5 be made conductive and the N-channel IGFETs 3, 4, 8 and 9 be made non-conductive. As has been explained above, the voltage-to-current converters and the active loads "remember" their currents after the N-channel IGFETs 3, 4, 8 and 9 are made non-conductive, so the conditions in the voltage comparator are substantially unaffected by the IGFETs 3, 4, 8 and 9 becoming non-conductive. The change in the condition of the N-channel IGFET 5 to its conductive state results in the equalisation of the charges stored by the gate electrodes of the IGFETs 1 and 6, a change in the drain currents of the IGFETs 1 and 6, and a change in the difference between the voltages present at the output ports 14 and 15. The voltage at one output port rises and the voltage at the other output port falls, the rise being equal in magnitude to the fall (because the average value of IN1 and IN2 will be $(\frac{IN1 + IN2}{2})$. The rise and fall of the voltages at the output ports 14 and 15 have the greatest effect on the IGFETs 10 and 11 since their gate electrodes are connected to those ports and the IGFETs 2 and 7 are now acting as high dynamic impedance "current memories".

There is now enough gain to make the bistable latch consisting of the IGFETs 10 and 11 regenerative and to switch to a condition determined by the sense of the voltage change at the output ports 14 and 15, and that voltage change includes no offset voltage component.

Referring to Fig. 1, if the input voltages are IN1a and IN2a immediately before the equalisation of the charges at the gate electrodes of the IGFETs 1 and 6, and these input voltages are IN1b and IN2b immediately after that equalisation, where IN1b, in fact, is equal to IN2b, then the change in output voltage is:

[gain (IN1b - IN2b + offset)] - [gain x (IN1a - IN2a + offset)]

which is equal to gain x (IN1a - IN2a) since IN1b = IN2b. The expression gain x (IN1a - IN2a) is the change in the output voltage and includes no offset term.

In practice, the N-channel IGFETs 3, 4, 8 and 9 are operated by a first clock signal which switches them alternately on and off, and the N-channel IGFET 5 is operated by a second clock signal which switches it alternately on and off, the first and second clock signals being in anti-phase to each other.

The voltage comparator represented By Fig. 1 is especially suitable for use in flash analogue to digital converters using a digital CMOS fabrication process. This voltage comparator is capable of providing an output which is very little affected by offset voltage, because it is operable to provide offset voltage reduction, is

fast in operation, because the latch which stores the result of the comparison is a positive feedback system with exponentially increasing gain, has good rejection of power supply noise, because the circuit symmetry ensures that differential voltages are not influenced by power supply noise, has very little charge injection at either input port, because there are open switches at the input ports when the result of the comparison is being determined, and is compact, because no capacitors are required to achieve offset reduction.

Referring to Fig. 1, the output rises exponentially with a time constant which can be expressed as:

$$t = \frac{K \times [\text{gate length}]^2}{\text{effective channel mobility} \times [V_{gs} - V_{th}]}$$

where the parameters are all for the latch IGFETs 10 and 11, V_{gs} and V_{th} being, respectively, the gate-source operating and threshold voltages for those IGFETs. Since the operating speed is dependent on the output time constant it is desirable to have short gate length IGFETs (of the order of 6 μm), large quiescent (V_{gs} - V_{th}), and high effective channel mobility. Very fast clock drivers are most effective for driving the comparator because there is some charge injection from the switches. The effect of the charge injection on circuit voltages has an exponential relationship to the clock rise and fall times and, also, to the clock skew, so these undesired effects can be reduced by increasing the clock edge speed.

Fig. 2 shows the right hand (as viewed) voltage-to-current converter and active load of the voltage comparator of Fig. 1. As has been described above with reference to Fig. 1, with a voltage V_{DD} applied directly to the source electrode of the IGFET 6, or applied through a current source, the source electrode of the IGFET 7 grounded, a signal voltage IN2 applied to the input port 13, and the IGFETs 8 and 9 switched on, that is, conductive, a current, substantially dependent on IN2 alone is established through the IGFETs 6 and 7. The IGFET 7 develops the correct gate voltage for it to pass the current supplied and the common drain voltage of the IGFETs 6 and 7 and the gate voltage of the IGFET 7 (which is the same as the common drain voltage of the IGFETs 6 and 7) is established by the devices. When the IGFETs 8 and 9 are switched off, that is, non-conductive, the signal voltage IN2 is stored on the gate electrode of the IGFET 6; also, the common drain voltage of the IGFETs 6 and 7 is stored on the gate electrode of the IGFET 7 as its gate voltage, with the result that the current flowing in the IGFETs 6 and 7 is maintained, or "remembered", after the removal of the signal IN2. If the charge stored on the gate electrode of the IGFET 6 is altered, that change is reflected as a change in the common drain voltage of the IGFETs 6 and 7, since the IGFET 7 will attempt to maintain its current at the original value. The IGFETs 7 and 9, therefore, form a current memory and is useful as a part of a voltage

comparator, for example, as described above.

As will be evident from Fig. 1 and 2, the voltage comparator described above avoids the need for a capacitor dedicated to storing an offset signal, so any additional processing steps for providing such a capacitor are avoided. This comparator fabricated as an integrated circuit could be smaller than a conventional comparator by an amount equal to the relatively large areas that a dedicated capacitor requires.

Also, in comparison with the voltage comparator represented by Fig. 1, known comparators have poor rejection of power supply noise, low input impedance at one of the input ports during the comparison phase, and require many stages to achieve the high gains needed for high-speed operation (they lack the regeneration of the latch stage used in this comparator). This voltage comparator does not require a separate step for offset storage as the offset is dealt with in the same step as that in which an output signal is provided.

CLAIMS:

1. A voltage comparator which is operable to provide an output signal indicating which of two voltages supplied to its input ports is the greater, by the steps of:

generating, by means of voltage-to-current converts, respective first and second currents corresponding to the two applied voltages,

applying the first and second currents to respective active loads which are capable of being set to maintain operation at those currents,

setting the active loads to maintain operation at the first and second currents,

applying to the voltage-to-current converters, in place of the two applied voltages, a common input voltage that is the means of the two applied voltages,

generating substantially equal currents corresponding to the common input voltage,

applying the substantially equal currents to the active loads in place of the first and second currents, the active loads being set to conduct the first and second currents, and

providing an output signal indicating the sense of any voltage change occurring at the active loads when the substantially equal currents are applied in place of the first and second currents.

2. A voltage comparator as claimed in claim 1, wherein

a regenerative switching circuit is connected between the active loads for providing an output signal indicating the sense of any voltage change occurring at the active loads when the substantially equal currents are applied in place of the first and second curents.

3. A voltage comparator as claimed in claim 2, wherein the regenerative switching circuit is a bistable latch circuit.

4. A voltage comparator as claimed in claim 3, wherein the bistable latch circuit consists of a first and a second insulated gate field effect transistor (IGFET), the gate electrode of the first IGFET being connected to the drain electrode of the second IGFET and to one of the active loads, and the gate electrode of the second IGFET being connected to the drain electrode of the first IGFET and to the other active load.

5. A voltage comparator as claimed in any one of claims 1 to 4, wherein each active load is a voltage-controlled current sink that is operable, first, to generate its own control voltage in order to conduct a current applied to it, and is then operable in a state in which it stores and responds only to the control voltage generated while it conducted the applied current.

6. A voltage comparator as claimed in claim 5, wherein

the voltage-controlled current sink includes an IGFET which has its gate electrode connectible to its drain electrode by way of a switch means.

7. A voltage comparator as claimed in any one of claims 1 to 6, which has a first input port connectible to a control port of a first voltage-to-current converter by way of first switch means, a second input port connectible to a control port of a second voltage-to-current converter by way of second switch means, the control ports of the voltage-to-current converters being capable of storing charge and being connectible together by third switch means, in operation, the first and second currents being generated with the third switch means non-conductive and the first and second switch means conductive, and the substantially equal currents being generated with the third switch means conductive and the first and second switch means non-conductive.

8. A voltage comparator substantially as herein described with reference to, and as illustrated by, Fig. 1 of the accompanying drawings.

9. An analogue-to-digital converter including a voltage comparator as claimed in any one of claims 1 to 8.

10. A circuit arrangement including a voltage-to-current converter connected to supply current to an active load,

wherein the active load is a voltage-controlled current sink operable, first, to generate its own control voltage in order to conduct a current applied to it, and is then operable in a state in which it stores and responds only to the control voltages generated while it conducted the applied current.

11. A circuit arrangement as claimed in claim 10, wherein the voltage-controlled current sink includes an IGFET which has its gate electrode connectible to its drain electrode by way of a switch means.

12. A circuit arrangement substantially as herein described with reference to, and as illustrated by, Fig. 2 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

(i) UK Cl (Edition K) H3W (WAC,WVP)

(ii) Int Cl (Edition 5) H03F 3/45

Search Examiner
D MIDGLEY

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search
31.10.01

Documents considered relevant following a search in respect of claims 1-9

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
	NONE	

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

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